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Implementation and Determining Low Power Analysis of Various Structures of SRAM Cell

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***Abstract*—The Reduction of the channel length due to scaling increases the leakage current resulting in a major contribution to the static power dissipation and for stability of the SRAM cell good noise margin is required so noise margin is the most important parameter for memory design. The higher noise margin of the cell confirms the high-speed of SRAM cell. In this work, SRAM Cell with six transistors is being proposed to reduce the static hence total power dissipation. When compared to the conventional 6T SRAM, 7T, 8T, 9T, 10T_SRAM cell and the proposed modified 6T SRAM with stack operation shows a significant reduction in the gate leakage current, static and total power dissipation while produce higher stability. In the technique employed for the proposed SRAM cell, the aim is to reduce the leakage power, leakage current and improve the read behavior of the different SRAM cell structure for 64 bit using cadence tool at 180nm technology while keeping the read and write access time and the power as low as possible analyzed by normal simulation and mote carlo simulation.**

***Index Terms*— Semiconductor Memories, Stack operation, CMOS t, Monte Carlo simulation.**

I. INTRODUCTION

The word memory recognizes data (digital information necessary to all systems) storage that arrives in the form of electronic device or tapes or disks. The terminology memory widely employs a short hand for physical memory. This refers to the concrete chips able of storing information. The quantity of memory requisite for a meticulous approach relies on the sort of the applications [1]. However, the count of transistors required in the task of data storage is relatively bigger as compared to count transistors required for logical action and other function.

In the current era the entire thing is computerized and there is an essential to categorize and development of immensity of information which desires to be processed at the request, and take place the multi tasking necessitate. In charge to handle with these problems, there require a well organized memory structure, particularly in the domain of VLSI design. These provisions formulate memories into publicity of research. At the same time as considering on memories there are different types, according to the requirement [5]. Random Access Memory (Ram) acts a fundamental role on various VLSI applications. The two important types of memory that perform a critical role in the VLSI memory are static random access memory (SRAM) and dynamic random access memory (DRAM).

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II. PROPOSED METHODOLOGY

This paper intends a novel design, which refer to as segmented Virtual Grounding or stacking operation which directs both dynamic and static power consumption. By introduction of stack operation, the bit lines are selectively discharged depending on where they are selected or not. This technique reduces the dynamic power consumption .in the proposed architecture selective variation of the source voltage of the drive transistors breaks the deadlock between the standby power utilization and utilization of dynamic power [2]. The data stability affects the SRAM cell due to reduction of supply voltage of bit cell of memory. It is shown that dynamic data stability of the SRAM cell opens a Broad opportunity for low power SRAM design as well as design for test.

A. SRAM cell

Memory cells are the key components of any SRAM unit. The SRAM unit .The SRAM memory cell has capacity of storing one bit of data [4]. SRAM cell has two end-to-end coupled inverters which forms a latch and has two access nmos pass transistors. Access pass transistors serve for both read and write retrieve to the memory unit. A static RAM offers the following basic properties:
Retention: The SRAM cell has the capacity for holding data indefinitely only if memory cell is power – driven.
Read: Read operation of static Ram is able to pass on data which is written to bit cell this operation doesn't changes information.
Write: the data of an SRAM Cell is able to write either of two values one or zero regardless of its original data.
Different types of SRAM cell topologies is been accounted over last ten year [3]. Between different topologies, 4_T static Ram with load resistance, 4_T structure without load as well as 6_T static Ram structure is certain with gradual loss of charge of pass transistor for this reason, these are not suitable candidates intended for low power applications. Alternatively, the data stability in a6 transistor SRAM cell is not dependent of leakage current. Moreover, the major advantage of 6_T topology shows considerably high tolerance against the noise. Figure 1. benefits especially in technologies with scaled devices in which noise margins are shrinking, which is main cause for popularity of low power SRAm for 6_T SRAm bit cell to 4_T configuration of SRAM cell.

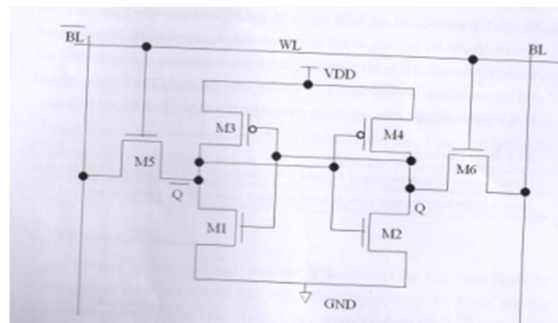

Figure 1. conventional 6T-Sram cell

B. Read operation

During access of read procedure of static RAM unit is shown in fig. from figure at point A holds logic 0 and at point B holds a value 1 prior to cell is being accessed. Therefore the faded colored transistors M# and M^6 are inactive i.e. OFF but transistors M$ and M5 are active i.e. ON. Figure 2 shows the bit lines of cell are precharged to given supply voltage vdd1 prior to the start of read operation in typical SRAM design.
The operation commences when the word line 'WL' is being enabled. M2 enters into region of saturation when WL is made active; meanwhile M4 drives into triode region. At terminal A, transistor M2 current and voltage has linear characteristics due to the effect of short channel. Thus the behavior becomes resistor. Hence there forms a voltage divider with resistor M4 and Mm2, raises the voltage at point A with delta V. the inverter M5to M3 is being driven by delta V as input to the M5 and M3 inverter. With constant value of vdd for M4 terminal of gate allows invariable resistivity and fig illustrates the path for discharge of bit line as linear model. Thus the bit lines are precharged to supply voltage vdd.

When M2 is enabled, capacitance bit line ‘CBL’ discharges through M4 stays 0 i.e. Vgs=0, CBL is not discharged, stayed at vdd. Since the gate source voltage of M1 remains at zero volts vgs1=0CBL cannot discharge and remains at VDD. To obtain usual levels of logic sensamplifier is being used to amplify the BL and BLB differential voltages. Obviously, quick path discharge for bit line is being accomplished, by dropping resistance in the path of discharge. Conversely these enhancements arrive for bigger sizes of transistors. For large bulk sram these improvement are not recommended.

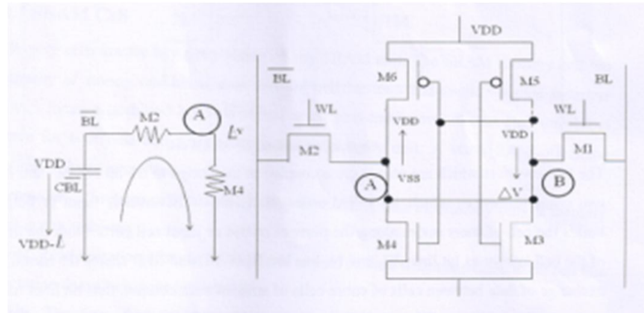

Figure 2.An SRAm cell during read operation (a) linear model of transistor involved in bit line discharge (b) cell status during read operation

C. Write operation

The operation of write process of SRAMunit is descrided in fig . From figure the terminals A and B are initially VSS and VDD correspondingly. Modifying previous information is insignificant in to the cell. Thus it is better to focus altering the cell data . it is noted that if the terminal A and B level of voltage turns to vdd and Vss then the write operatio process is completed. As it was specified in the past subsection,for an appropriate CR, the enabling of the wordline cannot bring a adequate voltage raise on terminal AQ to stimulate inverter M5 to M3 if both bitlines are precharged to Vdd. Subsequently operation of write is led by decreasing biot line connected to terminal BL and BLB to sufficiently low voltages Vss. By this process frames voltage divider consists of M5 and M1 towards the start of the operation. An adequately low delta voltage initiates inverter M6 to M4 results up charging terminals A with Vdd. Because terminal A operates inverter M5 to M3.terminal B is dragged to VSS through M3 and M5 turns ON consequently cell logic state is alteres. WL turns to dormant subsequent to termination of operation. Figure.3 shows An efficient write operation can be ensured by selecting appropriate PR. Lesser PR outcomes in lesser delta V connected with larger drive at the contribution of inverter M6 to M4. To accomplish lower PR wider access transistor is used. But by raising the access transistor width it causes cell stability during rsd operation by changing CR. Thus it entitles trade-off among data stability in the retrieving operation and write operation accomplishment. With the desired voltage of bitlines, desired sort offunction is important for memory cell. This requires external blocks such as buffer precharge circuit to provide suitable BL potential adjusting prior to any operation.

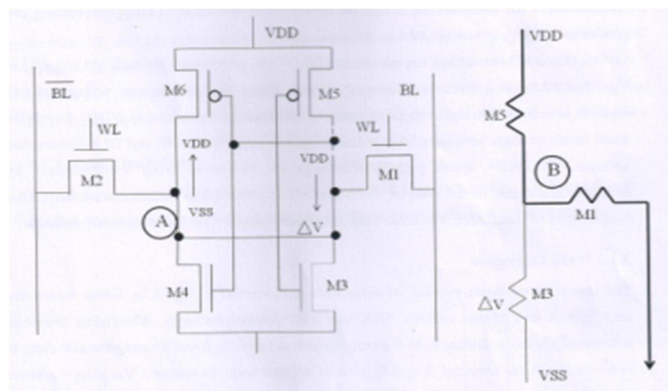

Figure.3 An SRAM cell during write operation (a) linear model of transistor that initiate the write operation (b) cell status during write operation

III. Experimental Work

Waveform is generated by using W-Edit. The transient response of various cells is given below shows the Simulation Results of various topologies.

Figure 4. Transient Response of 64 bit 6T SRAM Cell

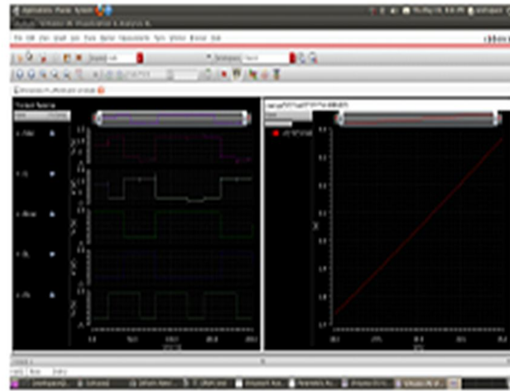

Figure 5. Transient Response of 7T SRAM Cell

Figure 6. Transient Response of 8T SRAM Cell.

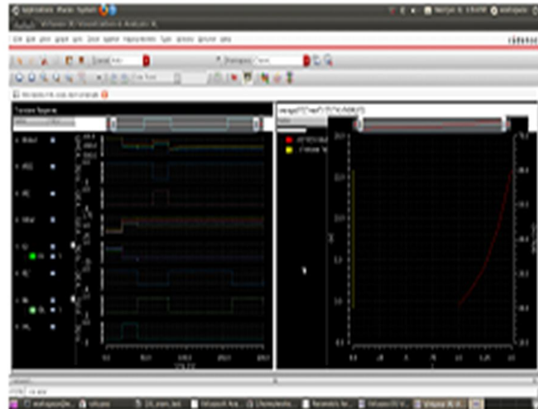

Figure 7. Transient Response of 8T SRAM Cell

IV. Comparative Analysis Using Various Parameters

From the above design and implementations, RAM has been compared on the basis of following parameters and its performance has been analyzed. The final results for the delay, power dissipation and SNM are shown in table I.

TABLE I. Performance parameter of various SRAM Cell Structure

SL. NO	Performance parameter	6T SRAM CELL	7T SRAM CELL	8T SRAM CELL	9T SRAM CELL	10T SRAM CELL	Modified 64 bit 6T SRAM
1	Technology	180nm	180nm	180nm	180nm	180nm	180nm
2	Supply voltage	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V
3	No. of NMOS transistor	2	2	2	2	4	2
4	No. of PMOS transistor	4	5	6	7	6	4
5	Power	43.73 uw	3.85 uw	43.82 uw	43.72 uw	43.92 uw	97.16 uw

For comparative analysis of 6T SRAM cell, 8T SRAM cell and 10T SRAM cell, hp0.5µm technology has been used . On the basis of NMOS transistor whose number is varying from 4,5,6 and PMOS transistor whose number is varying from 2,3,4 for 6T SRAM cell, 8T SRAM cell and 10T SRAM cell respectively, with the same supply voltage of 2.5V,it had been analyzed.

- For 6T SRAM cell-Keeping frequency 5MHz, it is found that power consumption is 1.25µW and delay is 3nsec.
- For 8T SRAM cell- Keeping frequency 8MHz, it is found that power consumption is 1.37µW and delay is 0.8nsec.
- For 10T SRAM cell- Keeping frequency 10MHz, it is found that power consumption is 1.487µW and delay is 0.5nsec.

From the above values, it can be concluded that the power consumption of 6T SRAM cell is lesser in comparison to 8T SRAM cell and10T SRAM cell whereas Static Noise Margin is highest for 6T SRAM cell and lowest for 10T SRAM cell. Also it can be seen that the stability will be highest in 6T SRAM cell than in comparison with 8T SRAM cell which is having medium and 10T SRAM cell which is having lowest stability. Thus 10T SRAM cell has lowest delay and SNM and thus achieves better performance as compared to 6T and 8T SRAM cell.

V. CONCLUSION

It has been concluded that if the number of transistor is increased in the SRAM cell the power dissipation will be increased due to increase in area, but other parameter like noise, delay can be reduced during read and write operation. So the optimum case is taken between speed, power and area.

REFERENCES

[1] Evelyn Grossar, Michele Stucchi, Karen Maex and Wim Dehaene "Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies" IEEE J. Solid State Circuits, vol. no. pp. 2577-2588,Nov. 2006.

[2] Jan M. Rabaey, Anantha chandrakasan, Borivoje Nikolic, "Digital integrated circuit A design perspective" second addition, Prentice Hall electronics and VLSI series. Berkley, Calistoga, ICSE 2008 Proc.2008, Johor Bahru, Malaysia Cambridge. 2003.

[3] Stefan Cosemans, Wim Dehaene and Francky Catthoor "A Low Power Embedded SRAM for Wireless Applications "IEEE J. Solid State Circuits, vol. 42, no. 7,pp. 1607- 1610 July 2007.

[4] K. Takeda, Y. Hagihara, Y. Aimoto, M. Nomura, Y. Nakazawa, T. Ishii, and H. Kobatake, "A Readstaticnoise-margin-free SRAM cell for low-VDD and highspeed applications," IEEE J. Solid-State Circuits, vol. 41, no. 1, pp. 113-121, Jan. 2006.

[5] Byung-Do Yang and Lee-Sup Kim "A Low Power SRAM using Hierrchical Bit Line and Local Sense Amplifiers" IEEE J. Solid-State Circuits, vol. 40, no. 6, pp. 1366- 1376, June 2005.

[6] Kouichi Kanda, Hattori Sadaaki, and Takayasu Sakurai "90% Write Power Saving SRAM Using Sense Amplifying Memory Cell" IEEE J. Solid-State Circuits, vol. 39, no. 6, pp. 927-933, June 2004.